8bit 12-channel D/A converter

BU2500FV / BU2501FV

BU2500FV / BU2501FV is a 12ch high-performance 8bit D/A converter which adopts the R-2R system.
The BU2500FV utilizes a 5V supply voltage and the BU2501FV a 3V. Each channel output incorporates a Rail to Rail output type buffer amplifier. Three wire serial data input and cascade connection is possible. Small package (0.65mm pitch and 20pin) is adopted.

●Applications

CD-R, CD-RW, DVC, Digital camera and industrial equipment

●Features

1) High-performance 8bit 12-channel D/A converter adopting the R-2R system.
2) Output of each channel incorporates a Rail to Rail output type buffer amplifier.
3) Digital input compatible with TTL levels.
4) 12bit 3wire serial data input, cascade connection is possible.
5) Buffer amplifier of each channel is highly-stable. Prevents oscillation even with capacitance loads.

●Absolute maximum ratings (Ta=25°C)

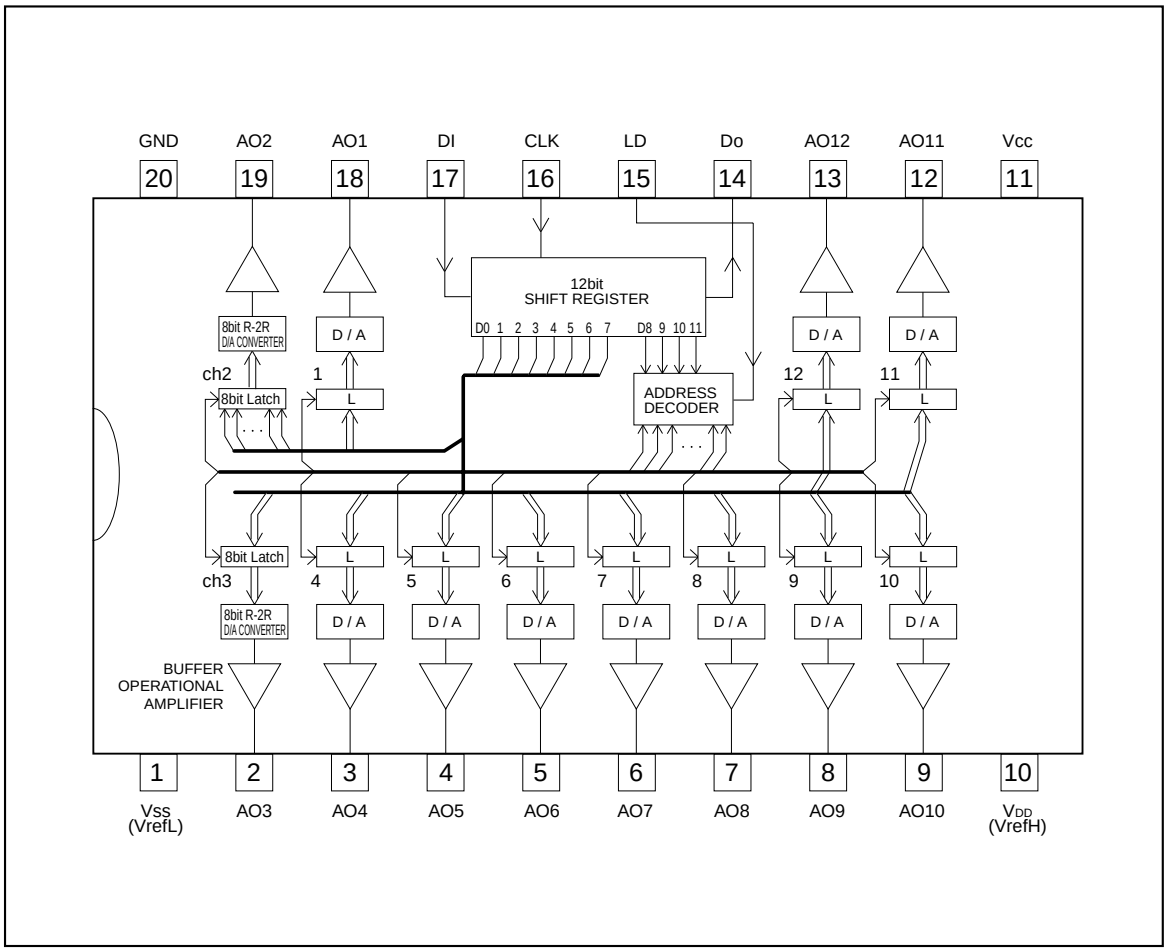
Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	−0.3~+6.0	V
Upper reference voltage of D/A converter	V_{DD}	−0.3~+6.0	V
Input voltage	V_{IN}	−0.3~+6.0	V
Output voltage	V_{OUT}	−0.3~+6.0	V
Power dissipation	Pd	400*	mW
Operating temperature	Topr	−25~+85	°C
Storage temperature	Tstg	−55~+125	°C

* Reduced by 4mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage (BU2500FV)	V_{CC}	4.5~5.5	V
Supply voltage (BU2501FV)	V_{CC}	2.7~3.6	V

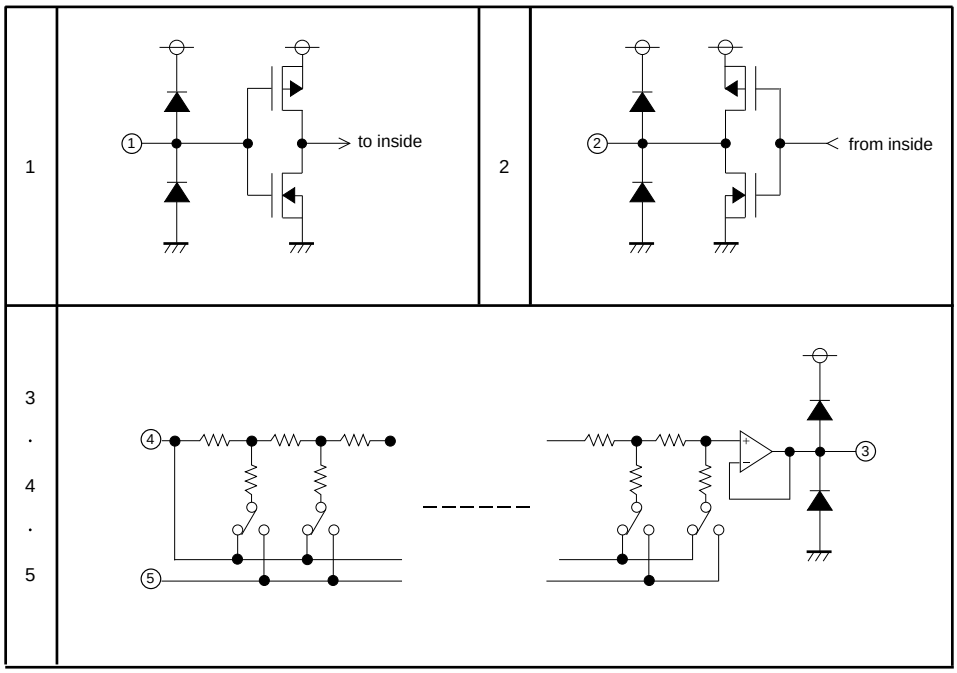
●**Block diagram**



●Pin descriptions

Pin No.	Pin name	Analog / Digital	I / O	Function	Circuit
1	Vss	Analog	–	D/A converter lower reference voltage input terminal	5
2	Ao3	Analog	O	8bit D/A converter output terminal (CH3)	3
3	Ao4	Analog	O	8bit D/A converter output terminal (CH4)	3
4	Ao5	Analog	O	8bit D/A converter output terminal (CH5)	3
5	Ao6	Analog	O	8bit D/A converter output terminal (CH6)	3
6	Ao7	Analog	O	8bit D/A converter output terminal (CH7)	3
7	Ao8	Analog	O	8bit D/A converter output terminal (CH8)	3
8	Ao9	Analog	O	8bit D/A converter output terminal (CH9)	3
9	Ao10	Analog	O	8bit D/A converter output terminal (CH10)	3
10	V_{DD}	Analog	–	D/A converter upper reference voltage input terminal	4
11	Vcc	–	–	Power supply terminal	–
12	Ao11	Analog	O	8bit D/A converter output terminal (CH11)	3
13	Ao12	Analog	O	8bit D/A converter output terminal (CH12)	3
14	Do	Digital	O	Terminal to output MSB data of 12-bit shift register	2
15	LD	Digital	I	When H-level signal is input to this terminal, the value stored in 12-bit shift register is loaded in decoder and D/A converter output register.	1
16	CLK	Digital	I	Shift clock input terminal. Input signal at DI pin is input to 12-bit shift register at rise of shift clock pulse	1
17	DI	Digital	I	Serial data input terminal to input 12-bit long serial data	1
18	Ao1	Analog	O	8bit D/A converter output terminal (CH1)	3
19	Ao2	Analog	O	8bit D/A converter output terminal (CH2)	3
20	GND	–	–	GND terminal	–

●Input / Output terminal equivalent circuits



●**Electrical characteristics**

• Digital characteristics

BU2500FV (unless otherwise noted, V_{CC}=5V, VrefH=5V, VrefL=0V, Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply current	I_{CC}	–	0.5	1.5	mA	CLK=1MHz operation, V_{CC}=5V, I_{AO}=0µA
Input leak current	I_{ILK}	−5	–	5	µA	V_{IN}=0~V_{CC}
Input voltage "L"	V_{IL}	–	–	0.8	V	
Input voltage "H"	V_{IH}	2.0	–	–	V	
Output voltage "L"	V_{OL}	0	–	0.4	V	I_{OL}=2.5mA
Output voltage "H"	V_{OH}	4.6	–	5	V	I_{OH}=−2.5mA

BU2501FV (unless otherwise noted, V_{CC}=3V, VrefH=3V, VrefL=0V, Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply current	I_{CC}	–	0.4	1.2	mA	CLK=1MHz operation, V_{CC}=3V, I_{AO}=0µA
Input leak current	I_{ILK}	−5	–	5	µA	V_{IN}=0~V_{CC}
Input voltage "L"	V_{IL}	–	–	0.48	V	
Input voltage "H"	V_{IH}	1.2	–	–	V	
Output voltage "L"	V_{OL}	0	–	0.4	V	I_{OL}=2.5mA
Output voltage "H"	V_{OH}	2.6	–	3	V	I_{OH}=−2.5mA

• Analog characteristics

BU2500FV (unless otherwise noted, V_{CC}=5V, VrefH=5V, VrefL=0V, Ta=25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Consumption current		IrefH	–	0.9	1.8	mA	VrefH=5V, VrefL=0V Data condition : Maximum current
D/A converter Upper reference voltage		VrefH	3.0	–	5	V	Reference voltage can not always be set to any value in this range, because it is restricted to the buffer amplifier output voltage range.
D/A converter Lower reference voltage		VrefL	0	–	1.5	V	
Buffer amplifier Output voltage range		V_{AO}	0.1	–	4.9	V	I_{AO}=±100μA
			0.2	–	4.8		I_{AO}=+500μA
Buffer amplifier Output drive range		I_{AO}	–1	–	1	mA	Upper saturation voltage=0.3V Lower saturation voltage=0.2V
Accuracy	Differential non-linearity error	S_{DL}	–1.0	–	1.0	LSB	VrefH=4.79V, VrefL=0.95V V_{CC}=5.5V (15mV / LSB) Without load (I_{AO}=+0)
	Non-linearity error	S_L	–1.5	–	1.5		
	Zero code error	S_{ZERO}	–2	–	2		
	Full scale error	S_{FULL}	–2	–	2		
Output capacitative load		C_O	–	–	10	μF	
Pull-up I/O-cell internal R value		R_O	–	5	15	Ω	

◎This product is not designed for protection against radioactive rays.

BU2501FV (unless otherwise noted, V_{CC}=3V, VrefH=3V, VrefL=0V, Ta=25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Consumption current		IrefH	–	0.6	1.2	mA	VrefH=3V, VrefL=0V Data condition : Maximum current
D/A converter Upper reference voltage		VrefH	2.1	–	3	V	Reference voltage can not always be set to any value in this range, because it is restricted to the buffer amplifier output voltage range.
D/A converter Lower reference voltage		VrefL	0	–	0.9	V	
Buffer amplifier Output voltage range		V_{AO}	0.1	–	2.9	V	I_{AO}=±100μA
			0.2	–	2.8		I_{AO}=+500μA, –200μA
Buffer amplifier Output drive range		I_{AO}	–0.3	–	1	mA	Upper saturation voltage=0.4V Lower saturation voltage=0.4V
Accuracy	Differential non-linearity error	S_{DL}	–1.0	–	1.0	LSB	VrefH=2.61V, VrefL=0.05V V_{CC}=2.76V (10mV / LSB) Without load (I_{AO}=+0)
	Non-linearity error	S_L	–1.5	–	1.5		
	Zero code error	S_{ZERO}	–2	–	2		
	Full scale error	S_{FULL}	–2	–	2		
Output capacitative load		C_O	–	–	10	μF	
Pull-up I/O-cell internal R value		R_O	–	5	15	Ω	

◎This product is not designed for protection against radioactive rays.

• AC characteristics

BU2500FV (unless otherwise noted, V_{CC}=5V, VrefH=5V, VrefL=0V, Ta=25°C)

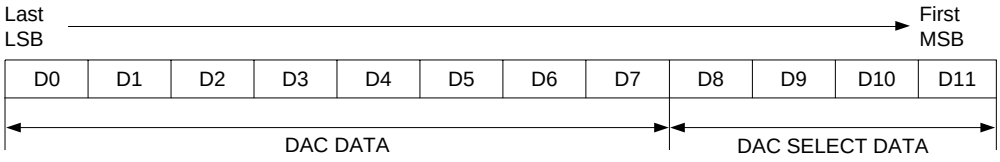
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock "L" pulse width	t_{CKL}	150	–	–	ns	
Clock "H" pulse width	t_{CKH}	150	–	–		
Clock rise time Clock fall time	tcr tcf	–	–	150		
Data set up time	t_{DCH}	20	–	–		
Data hold time	t_{CHD}	40	–	–		
LD set up time	t_{CHL}	150	–	–		
LD hold time	t_{LDC}	100	–	–		
LD "H" pulse duration	t_{LDH}	70	–	–		
Data output delay time	t_{DO}	70	–	350		CL=100pF
D/A output setting time	t_{LDD}	–	80	250	µS	CL≤1000pF V_{A0} : 0.5V⇔4.5V The time until the becomes the final value of 1/2 LSB.

BU2501FV (unless otherwise noted, V_{CC}=3V, VrefH=3V, VrefL=0V, Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock "L" pulse width	t_{CKL}	150	–	–	ns	
Clock "H" pulse width	t_{CKH}	150	–	–		
Clock rise time Clock fall time	tcr tcf	–	–	150		
Data set up time	t_{DCH}	20	–	–		
Data hold time	t_{CHD}	40	–	–		
LD set up time	t_{CHL}	150	–	–		
LD hold time	t_{LDC}	100	–	–		
LD "H" pulse duration	t_{LDH}	70	–	–		
Data output delay time	t_{DO}	70	–	350		CL=100pF
D/A output setting time	t_{LDD}	–	70	250	µS	CL≤1000pF V_{A0} : 0.1V⇔2.6V The time until the becomes the final value of 1/2 LSB.

●Circuit operations

• Data format



D0	D1	D2	D3	D4	D5	D6	D7	D/A output
0	0	0	0	0	0	0	0	(VrefH-VrefL) / 256×1+VrefL
1	0	0	0	0	0	0	0	(VrefH-VrefL) / 256×2+VrefL
0	1	0	0	0	0	0	0	(VrefH-VrefL) / 256×3+VrefL
1	1	0	0	0	0	0	0	(VrefH-VrefL) / 256×4+VrefL
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	(VrefH-VrefL) / 256×255+VrefL
1	1	1	1	1	1	1	1	VrefH

∗ VrefH=V_{DD} VrefL=V_{SS}

D8	D9	D10	D11	DAC selection
0	0	0	0	Don't Care
0	0	0	1	AO1 selection
0	0	1	0	AO2 selection
0	0	1	1	AO3 selection
0	1	0	0	AO4 selection
0	1	0	1	AO5 selection
0	1	1	0	AO6 selection
0	1	1	1	AO7 selection
1	0	0	0	AO8 selection
1	0	0	1	AO9 selection
1	0	1	0	AO10 selection
1	0	1	1	AO11 selection
1	1	0	0	AO12 selection
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

• Data timing

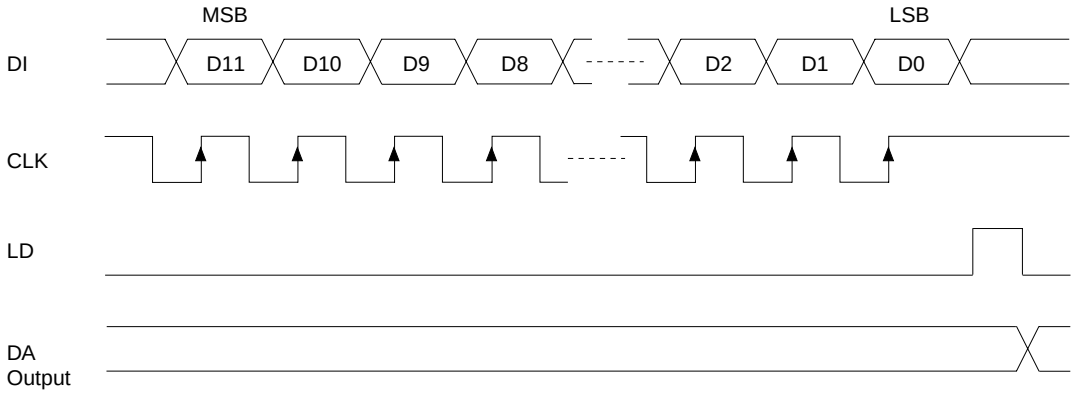


Fig.1

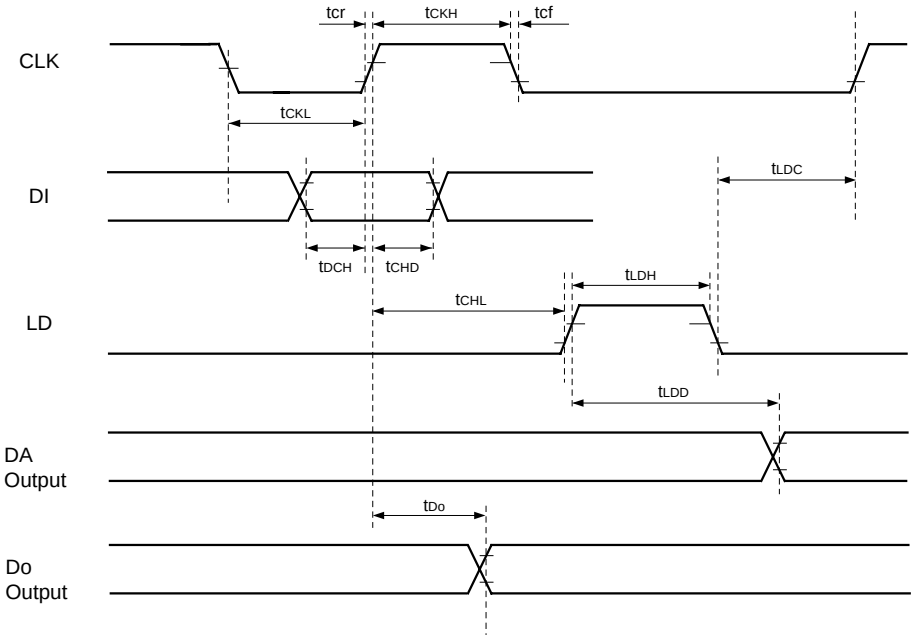


Fig.2

●**Application circuit**

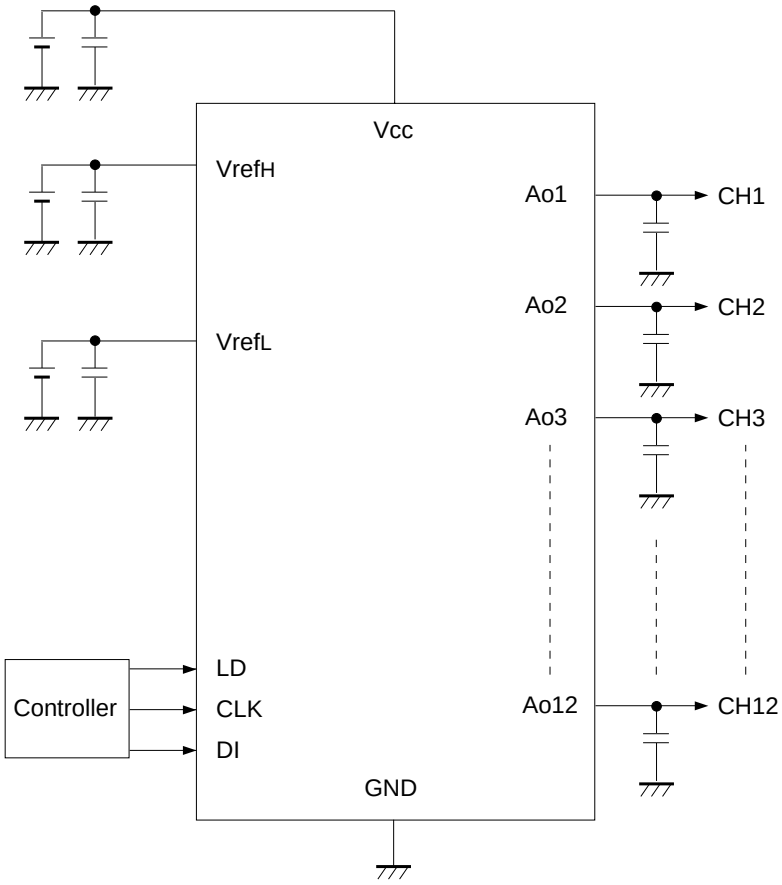


Fig.3

●**Operation notes**

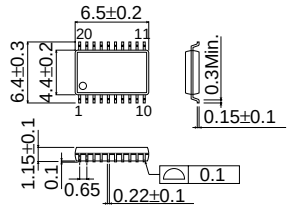
- There are 3 different type of power supply terminal and 1 type of GND terminal in this IC. Each of these terminals requires the constant power supply for operating.

- Pile up ripple and noise to these power supply terminals, it can't keep the accuracy of the D/A converter. Therefore external bypass capacitor recommend to set as close as possible to the terminals between VDD and GND in order to stabilizes the D/A converter.

- The capacitor between output and GND recommend to set under 100pF including parasitic capacitor in order to reduces jitter from layout of the output line and noise.

●**External dimensions** (Units : mm)

BU2500FV / BU2501FV



SSOP-B20